THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 26

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte ALBERT H. TADDIKEN and LUTZ J. MICHEEL

_____

Appeal No. 1997-1183
Application No. 08/066,362[1]

_____

HEARD: NOVEMBER 15, 1999

_____

Before THOMAS, GROSS, and DIXON, **Administrative Patent Judges**.

DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the Examiner's final rejection of claims 1-8. The examiner has indicated that claim 9 is allowable.

We AFFIRM-IN-PART - 37 CFR 1.196(b).

[1] Application for patent filed May 24, 1993.

BACKGROUND

The appellants' invention relates to multiple resonant tunneling circuits for signed digit multi-valued logic operations. Specifically, appellants' invention is directed to an adder of signed digit range-3 base-4 words using negative differential resistance devices. An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced below.

1. An apparatus for calculating the sum of two numbers, comprising:

signed digit range-3 base-4 words to represent said two numbers; and at least one device which exhibits negative differential resistance to calculate the sum.

The prior art references of record relied upon by the Examiner in rejecting the appealed claims are:

Singh 5,265,044 Nov. 23, 1993

Kawahito et al. (Kawahito), "Multiple-Valued Current Mode Arithmetic Circuits Based on Redundant Positive-Digit Number Representations", IEEE, pp. 330-339. (1991)

Kameyama et al. (Kameyama), "Modular Design of Multiple-Valued Arithmetic VLSI System using Signed-Digit Number System", IEEE, pp. 355-362. (1990)

Higgins,"Electronics with digital and analog integrated circuits", Chapter 9, Digital to Analog and Analog to Digital Conversion, pp. 288-289. Published by Prentice Hall, Inc., N.J. (1983).

Micheel et al. (Micheel), "Differential Multiple Logic Using Resonant Tunneling Diodes", Electronic Technology Laboratory (Wright-Patterson AFB, OH), pp. 1-7. (Date of publication unknown).

Claims 1-3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kameyama in view of (Singh or Micheel). Claims 1-4 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kawahito in view of (Singh or Micheel). Claims 5 and 6 stand rejected under 35 U.S.C. § 103 as being unpatentable over Kawahito and (Singh or Micheel) in view of Higgins. Claims 1-6 stand rejected under provisional obviousness-type double patenting over copending serial number 08/484,194. The examiner has withdrawn the rejection of claims 7 and 8 under 35 U.S.C. § 103 and double patenting. The examiner has also withdrawn the rejection of claims 1-3 under 35 U.S.C. § 112, first pargraph. (See answer at page 2.) The examiner has indicated that claim 9 is allowable. (**Id.**)

Rather than reiterate the conflicting viewpoints advanced by the Examiner and the appellants regarding the above-noted rejections, we make reference to the Examiner's answer (Paper No. 18, mailed July 12, 1996) and the letter (Paper No. 20, mailed November 1, 1996) for the Examiner's reasoning in support of the rejections, and to the appellants' brief (Paper No.16, filed April 8, 1996) and reply brief (Paper No. 19, filed Sep. 13, 1996) for the appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to the appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by the appellants and the Examiner. As a consequence of our review, we make the determinations which follow.

CLAIMS 1-4

With respect to the combination of Kameyama with (Singh or Micheel), appellants argue the references individually, asserting that "none of the references discloses the entire claimed invention." (See brief at page 7.) These arguments are not persuasive since the rejection is based upon the combined teachings of the references. Appellants further traverse the Examiner's conclusion that it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a negative differential resistance device in the parallel signed digit adder of Kameyama. We disagree with appellants. Appellants further argue that "[s]uch results [redundant encoded representations where ripple carries are never produced] are not obtained without the combination of the negative differential resistance devices and the sign redundant digit 4,3 coded [words], as required by the claims-in-issue. Such results are clearly unexpected." (See brief at pages 7-8.) We disagree with appellants. Clearly Kameyama teaches the skilled artisan that signed-digit adding reduces the carry propagation problem and increases speed of the manipulation. (See Kameyama at col. 1.) Kameyama discloses that the "carry propagation is always limited to one position to

the left" using redundant number representations and that it is applicable to radix 4 representations. (See Kameyama at page 356, col. 1.) Appellants provide no other evidence of unexpected results beyond the portion of the specification at page 7, lines 35-40 to support the above argument. This argument is therefore not persuasive since the prior art recognized the above elimination of carries with the sign redundant digit 4, 3 data.

With respect to Singh and Micheel, the Examiner relies upon each of these references to teach/disclose the well-known use of devices having negative differential resistance characteristics in logic circuits including summation functions. (See answer at page 3.) (See Micheel at page 1, col. 1 and Singh at abstract.) Micheel discloses the use of devices with negative differential resistance characteristics as beneficial for working at very high speeds and low propagation delays. (See Micheel at page 1, col. 1 and Singh at abstract.) Micheel further discloses the use of negative differential resistance devices for use in multiple valued logic. (See Micheel at abstract.) The Examiner maintains that it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the signed digit adder using at least one device which exhibits negative differential resistance as set forth in the language of claim 1. (See answer at page 3.) We agree with the Examiner.

As pointed out by our reviewing court, we must first determine the scope of the claim. "[T]he name of the game is the claim." ***In re Hiniker Co.***, 150 F.3d 1362, 1369,

47 USPQ2d 1523, 1529 (Fed. Cir. 1998). We find that the Examiner has provided a teaching or convincing line of reasoning why one skilled in the art would have desired to use negative differential resistance devices in multi-valued logic. Therefore, we conclude that the Examiner has provided a ***prima facie*** case of obviousness with respect to claim 1.

"To reject claims in an application under section 103, an Examiner must show an unrebutted prima facie case of obviousness. **See In re Deuel**, 51 F.3d 1552, 1557, 34 USPQ2d 1210, 1214 (Fed. Cir. 1995). In the absence of a proper prima facie case of obviousness, an applicant who complies with the other statutory requirements is entitled to a patent. **See In re Oetiker**, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). On appeal to the Board, an applicant can overcome a rejection by showing insufficient evidence of prima facie obviousness or by rebutting the prima facie case with evidence of secondary indicia of nonobviousness." **In re Rouffet**, 149 F.3d 1350, 1355, 47 USPQ2d 1453 (CAFC 1998). Here, we find that appellants have not overcome the ***prima facie*** case of obviousness by showing insufficient evidence by the Examiner of nonobviousness nor have appellants provided evidence of secondary indicia of nonobviousness. Therefore, we will sustain the rejection of claim 1.

With respect to the combination of Kawahito with (Singh or Micheel) applied against claims 1-4, appellants argue that "Kawahito does not disclose or suggest the

presently claimed invention including the at least one device which exhibits negative differential resistance to calculate the sum." (See brief at page 8.) This argument is directed to the individual reference rather than the combination of the teachings. Therefore, this argument is not persuasive. Since the Kawahito disclosure is similar to the disclosure of Kameyama, we will not repeat the above discussion. Therefore, we will sustain the rejection of claim 1 over the combination of Kawahito with (Singh or Micheel).

With respect to claims 2, 3 and 4, appellants have not presented separate arguments beyond paraphrasing the language of the claims. (See brief at page 9.) These arguments are not persuasive. Further, we note that the Examiner has directed appellants to Figure 5 of Kameyama to show the structure of the addition by direct connection and converter circuits to provide the output in the proper format and base (see answer at page 3) and to Figures 4 and 5 of Kawahito to show the structure of the addition by direct connection and converter circuits to provide the output in the proper format and base. (See answer at page 4.) Appellants have not rebutted this ***prima facie*** case of obviousness. Therefore, we will sustain the rejection of claims 2-4.

CLAIMS 5 AND 6

With respect to the rejection of claims 5 and 6, appellants argue that the prior art does not teach the "specific connection between two resonant tunneling multi-level

folding circuits." (See brief at page 9.) The Examiner relies on Kawahito to teach two resonant tunneling multi-level folding circuits with current sources and then substitutes Higgins' teaching of a voltage divider for the current sources. (See answer at pages 4-5.) The Examiner has not addressed the specific language of claim 5 and the specific interconnection of the voltage divider, nor has the Examiner provided more than a mere conclusion why one skilled in the art would have been motivated to make such a modification to the prior art teachings. Therefore, we will not sustain the rejection of claim 5 nor its dependent claim 6.

OBVIOUS DOUBLE PATENTING

The application listed in the rejection of claims 1-6 under provisional obviousness-type double patenting has been abandoned, therefore this issue is MOOT.

REJECTION UNDER 37 CFR 1.196(b)

The Examiner stated in the final rejection that claims 7 and 8 were similar to claims 4-6 and that a similar rejection applied to claims 7 and 8. In the answer the Examiner withdrew a rejection of claims 1-3 under 35 U.S.C. § 112, first paragraph and rejections of claims 7-9 under 35 U.S.C. § 103 and obvious type double patenting without stating a reason for doing so. (See answer, page 2). However, we agree with the Examiner's previous statement that claims 4 and 7 are similar. Therefore, we enter a rejection to claims 7 and 8 under 37 CFR 1.196(b).

Claims 7 and 8 are rejected under 35 U.S.C. § 103 over Micheel, Kawahito and Kameyama. Claims 7 is rejected as discussed above with respect to claim 4 as set forth thereto by the Examiner. We apply Micheel as the primary teaching since Micheel clearly teaches and suggests the use of resonant tunneling diodes (negative differential resistance devices) in multi-valued logic, as discussed above. Furthermore, we have included both Kameyama and Kawahito in the combination since both teach various embodiments of summation logic circuits which a skilled artisan would have realized would have benefited from the use of negative differential resistance devices in the processing circuitry. The motivation for the combination of the teachings would have been to further increase the speed of math processing of Kawahito (figures 4 and 5) and Kameyama (figure 5 and equations (1) -(6)) by using negative differential resistance devices. Furthermore, we note that there is a difference between the nomenclature used in the claim when compared to the references, but also note that they are functionally equivalent in the mathematical processing and conversion back to base 3 from base 5.

Claim 8 is rejected on the same basis as claim 7 further in view of the teaching of Kawahito which teaches the use of current states with increments of 0.5. (See Kawahito at page 336, col. 1 and figure 5.) Therefore, skilled artisans would have been motivated to use 0.5 as the line to separate the two lowest states.

CONCLUSION

To summarize, the decision of the Examiner to reject claims 1-4 under 35 U.S.C. § 103 is affirmed; the decision of the Examiner to reject claims 5-6 under 35 U.S.C. § 103 is reversed; and the decision of the Examiner to reject claims 1-6 under provisional obviousness-type double patenting is moot.

In addition to affirming the Examiner's rejection of claims 1-4, this decision contains a new ground of rejection pursuant to 37 CFR § 1.196(b)(amended effective Dec. 1, 1997, by final rule notice, 62 Fed. Reg. 53,131, 53,197 (Oct. 10, 1997), 1203 Off. Gaz. Pat. & Trademark Office 63, 122 (Oct. 21, 1997)). 37 CFR § 1.196(b) provides, "A new ground of rejection shall not be considered final for purposes of judicial review."

Regarding any affirmed rejection, 37 CFR § 1.197(b) provides:

> (b) Appellant may file a single request for rehearing within two months from the date of the original decision . . . .

37 CFR § 1.196(b) also provides that the appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of proceedings (37 CFR § 1.197(c)) as to the rejected claims:

> (1) Submit an appropriate amendment of the claims so rejected or a showing of facts relating to the claims so rejected, or both, and have the

> matter reconsidered by the Examiner, in which event the application will be remanded to the Examiner. . . .
>
> (2) Request that the application be reheard under § 1.197(b) by the Board of Patent Appeals and Interferences upon the same record. . . .

Should the appellants elect to prosecute further before the Primary Examiner pursuant to 37 CFR § 1.196(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the prosecution before the Examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If the appellants elect prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART - 37 CFR 1.196(b)

JAMES D. THOMAS Administrative Patent Judge	)))))) BOARD OF PATENT) APPEALS) AND) INTERFERENCES))))
JOSEPH L. DIXON Administrative Patent Judge	
ANITA PELLMAN GROSS Administrative Patent Judge	

vsh

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